

Appln No. 10/815,627
Amdt. Dated July 3, 2006
Response to Office Action of June 15, 2006

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Amendments to the Specification:

AC
8/28/06
The paragraph beginning at page ²⁵23, line 21 to line 27, is to be amended as follows:

Various netpage coding schemes and patterns are described in the present applicants' co-pending US application USSN 09/575154 entitled "Identity-Coded Surface with Reference Points", filed 23 May 2000; co-pending US application USSN 10/120441 entitled "Cyclic Position Codes", filed 12 April 2002; co-pending US application USSN 10/309358 entitled "Rotationally Symmetric Tags", filed 4 December 2002; co-pending US Application USSN 10/409864 entitled "Orientation-Indicating Cyclic Position Codes", filed 9 April 2003; and co-pending US Application USSN ~~10/786,631~~ 10/786,631 entitled "Symmetric Tags", filed 4 March 2004 (~~Docket number NPT037~~).

AC
8/28/06
The paragraph beginning at page ²⁹27, line 29 to line 31, is to be amended as follows:

Figure 54 shows the logical layout of another alternative hexagonal tag. This tag design is described in detail in the present applicants' co-pending US application USSN ~~10/786,631~~ 10/786,631 entitled "Symmetric Tags" (~~docket number NPT037US~~).

The paragraph beginning at page 86, line 4-7, is to be amended as follows:

The imaging unit incorporates both the image sensor 2412 and the image processor 2410, which are usefully combined into a single compact chip as described in the co-pending US applications USSN ~~10/778,056~~ 10/778,056 entitled "Image Sensor with Digital Framestore" (~~docket no. NPS047 US NPS054~~), USSN 10/778,058 entitled "Image Sensor with Low-Pass Filter", USSN 10/778,060 entitled "Image Sensor with Range Expender", USSN 10/778,059 entitled "Pixel Sensor", USSN 10/778,063 entitled "Image Sensor Timing Circuit", USSN 10/778,062 entitled "Image Processor with Low Power Mode", USSN 10/778,061 entitled "Image Processor", and USSN 10/778,057 entitled "Synchronization Protocol" filed 17 February 2004.